## CLAIM LISTING

No claims have been amended, canceled, or added. A Claim Listing is provided as a courtesy.

Claims 1-18 (Canceled).

19. (Previously Presented) A device comprising:

first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller, the first circuitry comprising:

second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in first-in first-out (FIFO) circuitry; and

third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO circuitry.

20. (Previously Presented) The device of claim 19, wherein the second circuitry comprises:

logic to synchronize receipt of the packet header from the micro-engine and the packet payload from the memory controller, to store the packet header in the FIFO circuitry, and to transfer the packet header and packet payload data from the FIFO circuitry to a destination specified in the packet header.